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(71) Applicant(s):
Advanced Micro Devices, Inc
(Incorporated in USA - Delaware)
One AMD Place, Mail Stop 68, Sunnyvale,
California 94088-34,
United States of America

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(56) Documents Cited by ISA:
IEEE Journal of Solid-State Circuits, Vol. 26, No. 11, November 2001, pp. 1617-1627
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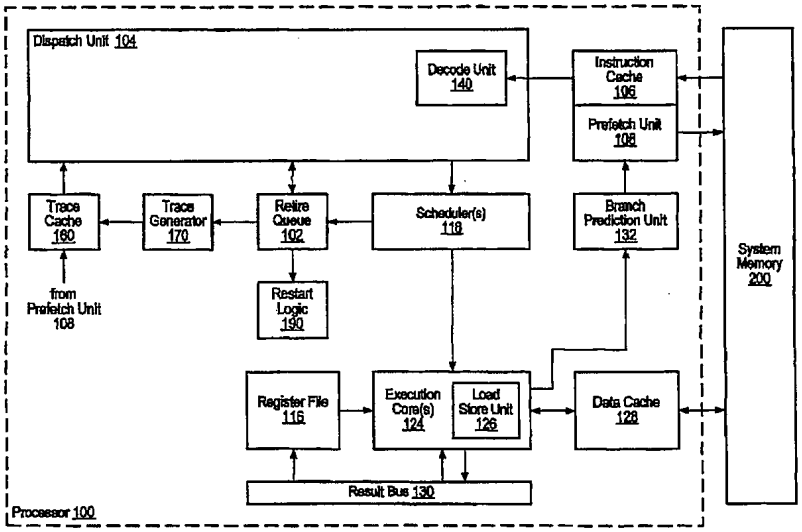
(54) Abstract Title: **System and method for handling exceptional instructions in a trace cache based processor**

(57) A system may include an instruction cache (106), a trace cache (160) including a plurality of trace cache entries (162), and a trace generator (170) coupled to the instruction cache (106) and the trace cache (160). The trace generator (170) may be configured to receive a group of instructions output by the instruction cache (106) for storage in one of the plurality of trace cache entries (162). The trace generator (170) may be configured to detect an exceptional instruction within the group of instructions and to prevent the exceptional instruction from being stored in a same one of the plurality of trace cache entries (162) as any non-exceptional instruction.



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(72) Inventor(s):
Mitchell Aisup
Gregory William Smaus
James K Pickett
Brian D McCinn
Michael A Filippo
Benjamin T Sander

(74) Agent and/or Address for Service:
Brookes Batchellor LLP
102-108 Clerkenwell Road, LONDON,
EC1M 5SA, United Kingdom